Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **GND**
2. **INPUT +**
3. **INPUT –**
4. **V –**
5. **BALANCE**
6. **BALANCE/STROBE**
7. **OUTPUT (2 pads)**
8. **V +**

**.045”**

**.065”**

**2 1 8 7**

**5 6 7**

**3**

**4**

**DIE ID**

**NOTE: Chip back must be connected to V -**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .045” X .065” DATE: 11/9/21**

**MFG: NATIONAL THICKNESS .015” P/N: LF111**

**DG 10.1.2**

#### Rev B, 7/1